

CLAIMS

1. A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs
5 intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting point between the plurality of match line pairs and the plurality of search line pairs, wherein

the plurality of match line pairs have precharge circuits;

10 the plurality of precharge circuits drive a first match line of the match line pair to a first voltage and a second match line thereof to a second voltage lower than the first voltage, respectively;

the plurality of memory cells have storage circuits and
15 comparators;

each of the comparators has a first and a second MOS transistors;

gate electrodes of the first and the second MOS transistors are connected to the plurality of search lines, respectively; and

20 either of source or drain electrodes of the first and the second MOS transistors are respectively connected to the plurality of first match lines.

2. The semiconductor integrated circuit device according to
25 claim 1, wherein

a source - drain path in the first MOS transistor is included in a first current path between the plurality search line pair;

a source - drain path in the second MOS transistor is included in a second current path between the plurality search line pair;

the comparator generates a signal voltage corresponding to a result obtained by comparing data held at the storage circuit and data inputted via the plurality of search lines at the plurality of match line pairs.

3. The semiconductor integrated circuit device according to claim 2, wherein

first and second coupling capacitances parasitic between the plurality of search line pairs and the plurality of first match lines are larger than third and fourth coupling capacitances parasitic between the plurality of search line pairs and the plurality of second match lines.

4. The semiconductor integrated circuit device according to claim 3, wherein

a plurality of match detectors are arranged in the plurality of second match lines, respectively; and

the plurality of match detectors determines the comparison result of data by discriminating voltages of the plurality of second match lines.

5. The semiconductor integrated circuit device according to claim 4, wherein

the storage circuit has two transistors and two capacitors.

6. A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs, wherein
5 the plurality of match line pairs have precharge circuits;
the plurality of precharge circuits drive a first match line of the match line pair to a first voltage and a second match line thereof to a second voltage lower than the first voltage,
10 respectively;
the plurality of memory cells have storage circuits and comparators;
the comparator comprises
first and second MOS transistors connected serially so as to
15 form a first current path between the plurality of match line pairs, and
third and fourth MOS transistors connected serially so as to form a second current path;
gate electrodes of the first and third MOS transistors are
20 connected to the plurality of search lines, respectively;
either of electrodes of source or drain electrodes of the first and third MOS transistors are connected to the plurality of first match lines through contacts formed through self-aligned process;
25 gate electrodes of the second and fourth MOS transistors are connected to the storage circuits, respectively; and
either of electrodes of source or drain electrodes of the second and fourth MOS transistors are connected to the plurality

of second match lines through contacts formed through self-aligning process.

7. The semiconductor integrated circuit device according to claim 6, wherein

first and second coupling capacitances parasitic between the plurality of search line pairs and the plurality of first match lines are generated principally by the contacts, respectively;

third and fourth coupling capacitances parasitic between the plurality of search line pairs and the plurality of second match lines are generated principally by an interlayer insulator formed between a first metal layer used for forming the plurality of search line pairs and a second metal layer used for forming the plurality of second match lines; and

the first and the second coupling capacitances are larger than the third and the fourth coupling capacitances.

8. The semiconductor integrated circuit device comprising a plurality of first match lines, a plurality of search line pairs intersecting the plurality of first match lines, a plurality of bit line pairs parallel to the plurality of search line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of first match lines with the plurality of search line pairs, wherein

the plurality of memory cells have storage circuits and comparators;

the storage circuits are connected to the plurality of bit line pairs;

the comparators are connected to the plurality of search line pairs and the plurality of first match lines; and

voltage amplitudes of the plurality of bit line pairs are larger than those of the plurality of search line pairs.

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9. The semiconductor integrated circuit device according to claim 8, further comprising a plurality of second match lines parallel to the plurality of first match lines, wherein

a plurality of match line pairs formed in a paired manner by the plurality of first match lines and the plurality of second match lines have precharge circuits;

the plurality of precharge circuits drive the first match lines of the match line pairs to a first voltage and the second match line of the match line pairs to a second voltage lower than the first voltage, respectively; and

the comparators are inserted between the plurality of match line pairs, and generate a signal voltage corresponding to a result obtained by comparing data held in the storage circuit and data inputted via the plurality of search lines at the plurality of match line pairs.

10. The semiconductor integrated circuit device according to claim 9, wherein

each of the storage circuits has two transistors and two capacitors.